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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,044	03/01/2004	Chung-Hui Chen	TSMC2003-0817(N1280-00070	1265

54657 7590 03/10/2006

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,044	CHEN, CHUNG-HUI	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-18 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-18 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-13, 15-18 and 20 are objected to because of numerous informalities:

Claim 1, line 16, "or" should be changed to --and-- (because "at least one of A or B" is grammatically incorrect).

Claim 1, line 16, "module" should be changed to --modules--.

Claims 2-6 are objected because they include the informalities of claim 1.

Claim 7, line 13, "or" should be changed to --and--.

Claim 7, line 13, "module" should be changed to --modules--.

Claims 8-11 are objected because they include the informalities of claim 7.

Claim 12, line 23, "or" should be changed to --and--.

Claim 12, line 23, "modules" should be changed to --module--.

Claim 13 is objected because it includes the informalities of claim 12.

Claim 15, line 20, "or" should be changed to --and--.

Claim 15, line 20, "modules" should be changed to --module--.

Claims 16-18 and 20 are objected because they include the informalities of claim 15.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 7-9, 15-18, 21, 22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki (US 5,081,373).

With respect to claims 1, 2, 4, 7, 9, 15-17, 21, 22 and 24, Figure 1 of the Suzuki reference discloses a flip-flop, which includes: a first pass gate (111); a clock signal (ø) and an inverted signal (ø/) of the clock signal (ø); an input (DI); a second pass gate (121; a first signal passing module (131, 141); a third pass gate (123l); a second signal passing module (132, 142); a fourth pass gate (113); and a driver module (inverter 151); wherein at least one of the first and the second signal passing modules is a NAND gate for receiving a flag signal (PST) and a respective passed input (outputs of 111, output of 121) passed by the first and second pass gates (i.e., the combination of AND 131 and inverter 141 is a NAND gate, and the combination of AND 132 and inverter 142 is also a NAND gate when signal RST is not used since elements 141 and 142 are inverters when signal RST is not used, see Col. 8, lines 22-29 for the case when signal RST is not used then an inverter is used in placed of each of the NOR gates 141 and 142). Note that although the symbol of the tri-state inverters 111, 121, 123 and 113 shows only one clock (either ø or ø/), however, the each of the tri-state inverter is controlled by both of the clock signals ø and ø/ because the detail of the tri-state inverter must be have a transistor that is controlled by clock ø and another transistor controlled by the clock ø/ (see Figure 2 of U.S. Patent 5,654,659 issued to Asada for evidence that the symbol of a tri-state inverter shown only one clock, but the detail of the tri-state inverter also including the inverted clock).

Note for claims 3, 8 and 18, because these claims are indefinite as discussed above, so if passing modules (NAND gates, recited in the respective independent claims) are considered to

be inverters, then the NAND gates for the passing module of the prior art also meet the limitation that the passing modules are inverters.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 6, 10-13, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (USP 5,081,373) in view of Weste et al. (Principles of CMOS VLSI Design: A Systems Perspective, 1993, Addison-Wesley Publishing Company, 2nd edition, page 91).

With respect to claims 5, 6, 10, 11 and 20, the flip-flop in Figure 1 of Suzuki meets all the limitations of these claims except that each of the first to fourth pass gates comprises a PMOS transistor and an NMOS transistor connected in parallel. However, the Weste et al. discloses that a tri-state inverter is easily constructed by cascading a transmission gate with an inverter (see Figure 2.37(a), lines 1-2 of paragraph 2.7). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to implement each of the tri-state inverters (111, 123, 121, 113) in Figure 1 of Suzuki by cascading a transmission gate with an inverter as taught in Figure 2.37(a) of Weste et al. for the purpose of easy and simple in constructing the flip-flop circuit. Thus this modification/combination meets all the limitations of these claims, i.e., each of the first to fourth pass gates 111, 121, 123 and 124 comprising a PMOS transistor and an NMOS transistor connected in parallel (i.e., the PMOS and NMOS transistors of the transmission gate that is used to cascade with inverter to implement the tri-state inverter as

taught by Weste et al.). Note that, because each of the tri-state inverters in Figure 1 of Suzuki operates as an inverter when a Low logic signal is applied to the control terminal of the tri-state inverter and the tri-states inverter is in tri-state when a Hi signal is applied to the control terminal of the tri-state inverter, so the PMOS transistor of the first and fourth pass gates (111 and 113) is controlled by the clock signal ø (because a logic Low signal of the clock signal ø turns on the PMOS transistor) and the NMOS transistor of the first and fourth pass gates (111 and 113) is controlled by the inverted clock signal ø/ (because when clock ø = Low, then inverted clock ø/ = Hi to turn on the NMOS transistor); and the NMOS transistor of the second and third pass gates (121 and 123) is controlled by the clock signal ø (because the tri-state inverters 111 and 113 passing the input in complementary manner with the tri-state inverters 121 and 123, so when clock signal ø = Lo for the tri-state inverters 111 and 113 to pass the signal, then the clock signal ø = Lo controlled the gates of NMOS transistors of tri-states 121 and 123 to turn off the NMOS transistors of tri-states 121 and 123; and vice versa, when the tri-states 111 and 113 are in tri-state mode when clock signal ø = Hi, and the logic Hi of the clock signal ø turns on the NMOS transistors of tri-state inverters 121 and 123 so that tri-state inverters 121 and 123 pass the signal) and the PMOS transistor of the first and fourth pass gates (121 and 123) is controlled by the inverted clock signal ø/ (due the tri-state inverters 111 and 113 passing the signal in complementary manner with the tri-state inverters 121 and 123 for similar reasons as discussed).

With respect to claims 12-13 and 23, these claims are rejected for the same manner as discussed in the modification of claims 5, 6, 10, 11 and 20, i.e., the first to fourth pass gates, the first and second signal passing modules, the driver are read from Figure 1 of Suzuki in the same

manner as discussed in 102 rejection, and the PMOS and NMOS transistors of each of the first to fourth pass gates are from the transmission gate of Figure 2.37(a) of Weste et al. as discussed in the 103 rejection of claims 5, 6, 10, 11 and 20.

Response to Arguments

6. Applicant's arguments have been considered but are not persuasive.

Applicant argues that Suzuki does not disclose "wherein at least one of the first or the second signal passing module is a NAND gate". However, this argument is not persuasive because Suzuki clearly discussed (see Col. 8, lines 22-29) for the case when signal RST is not used then an inverter is used in placed of each of the NOR gates 141 and 142, so the combination of AND 131 and inverter 141 is a NAND gate, and the combination of AND 132 and inverter 142 is also a NAND gate when signal RST is not used.

Applicant also argues that the combination of AND gate and a NOR gate is not the functional equivalent as a NAND gate. However, this argument is not persuasive because Suzuki clearly discussed that when signal RST is not used then an inverter is used in placed of each of the NOR gates 141 and 142 (see Col. 8, lines 22-29), so the combination of an AND gate and an inverter (when signal RST is not used) functions as a NAND gate.

Applicant also argues that the flag signal of applicant invention is functionally different from the preset signal PST and reset RST signal inputs of Suzuki because in applicant invention, "the flag identifies the power status of the circuit to prevent leakage problems when the flip-flop is not in operation" while the signal PST of Suzuki is used to initialize the signal passing portion. However, this argument is not persuasive because the recitation "the flag identifies the power status of the circuit to prevent leakage problems when the flip-flop is not in operation" is not

recited in the claim, so for broadest reasonable interpretation, any signal is reasonable to be considered as a flag signal, and thus the signal PST in Suzuki is reasonable to be considered as a flag signal.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER